A POWER DISTRIBUTED AMPLIFIER USING CONSTANT-R NETWORKS

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Abstract

This paper describes the design, implementation and performance of a power distributed amplifier with a minimum gain of 5dB, input and output VSWR less than 1.5:1, and greater than 22dBm of 1dB compressed power over the 2 to 18GHz band. This amplifier makes use of several circuit design advances to improve both bandwidth and power capability and measures 1.0mm by 1.4mm (1.4 sq. mm).

Introduction

Examples of power distributed amplifiers are now becoming common in the literature (1,2,3). The primary objective of these designs is to incorporate large gate peripheries for high power capability while maintaining the wideband frequency response for which the distributed amplifier is well known. This, however, presents a dilemma as large gate periphery implies high capacitance per section while amplifier bandwidth is inversely proportional to capacitance. Three techniques are used to address this problem in the distributed amplifier shown schematically in figure 1. The most significant innovation of the design is that each section of the distributed amplifier is incorporated into a "constant-R network" (4,5) as opposed to the more traditional constant-K network which has been used in all monolithic distributed amplifiers to date.

Circuit Design

The constant-R network is represented in figure 1 by the boxes labeled "Bridged-Tee Coil". A theoretical comparison of the constant-R and constant-K networks is shown in figure 2 where a section of each network is individually analyzed. In both cases, the shunt capacitor represents the parasitic capacitance of the active device while the remaining elements must be

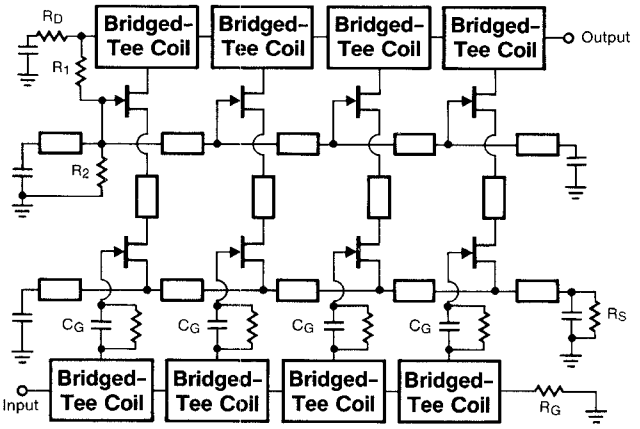

Figure 1. Schematic Diagram of the Distributed Amplifier

implemented external to the device. Under the conditions shown in the figure, the constant-R network becomes an all-pass network and presents a constant input impedance (R_L) which is independent of frequency (hence, the name, "constant-R"). A key parameter of these networks, when applied to distributed amplifiers, is the frequency at which the voltage across the shunt capacitor (FET) drops to $1/\sqrt{2}$ its low frequency value. This is known as the cutoff frequency. Note that for the same value of shunt capacitance the cutoff frequency for the constant-R network is a factor of $\sqrt{2}$ greater than that of the low pass constant-K network, which is a significant improvement.

The constant-R network contains three circuit elements that need to be implemented (apart from the shunt capacitance which is supplied by the FET): series inductance, mutual inductance and bridging capacitance. This network is implemented monolithically with the structure shown in figure 3a and modeled by the equivalent circuit of figure 3b. The coupled transmission lines provide the series and mutual inductance while the airbridge crossover provides the bridging

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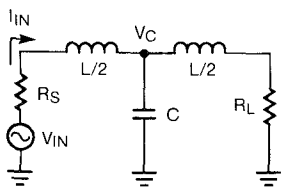
Constant-K



Conditions

$L = CR_L^2$

Transfer Function

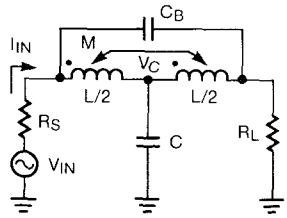
$$\frac{V_C}{I_{IN}} = \frac{2R_L + sR_LC}{2 + 2R_LCs + R_L^2C^2s^2}$$

Cutoff Frequency

$$f_C = \frac{1}{\pi\sqrt{LC}} = \frac{1}{\pi R_LC}$$

6dB/Octave Rolloff

Constant-R



Conditions

$L = 3CR_L^2/4 \quad M = CR_L^2/8 \quad C_B = C/8$

Transfer Function

$$\frac{V_C}{I_{IN}} = \frac{8R_L}{8 + 4R_LCs + R_L^2C^2s^2}$$

Cutoff Frequency

$$f_C = \frac{\sqrt{2}}{\pi R_LC}$$

12dB/Octave Rolloff

Figure 2. Theoretical Analysis of the Constant-K and Constant-R Networks

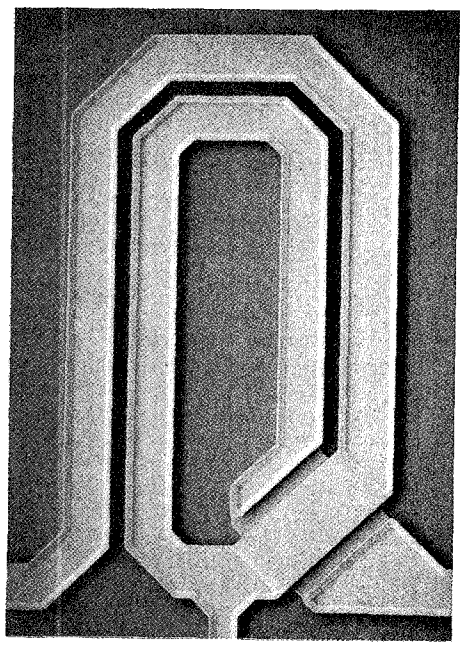


Figure 3a. SEM Micrograph of a Bridged-Tee Coil

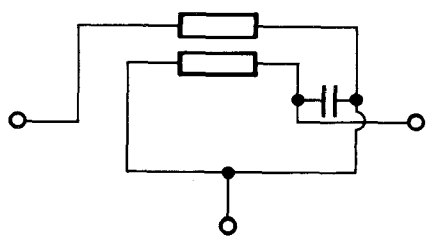


Figure 3b. Equivalent Circuit Model of the Bridged-Tee Coil

capacitance. Note that the circuit model of this structure differs from the ideal model of figure 2 in that coupled inductors are replaced with coupled transmission lines and the bridging capacitor is connected across only one of the coupled transmission lines. In practice, however, computer simulations of the distributed amplifier using the physical model of the constant-R network show a bandwidth improvement of 9GHz over the same design employing constant-K networks as shown in figure 4. Each simulation is based on a four section design using identical FET's which is optimized for maximum gain flatness and bandwidth.

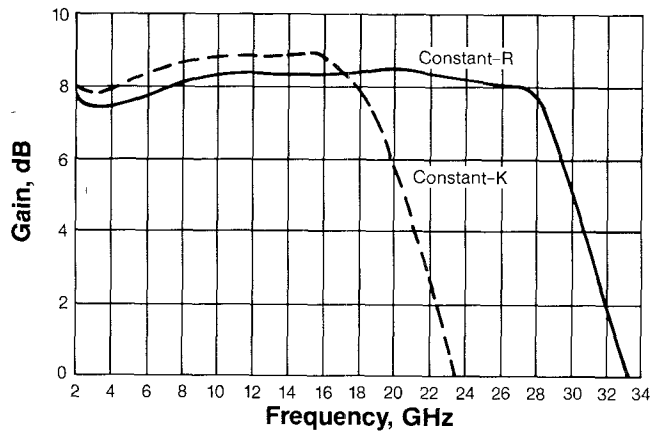


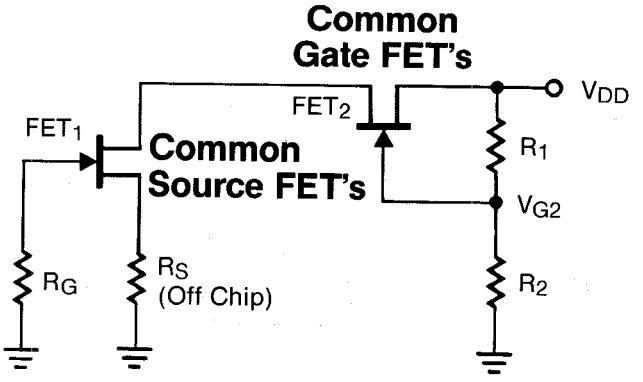
Figure 4. Simulated Gain Responses of Constant-K and Constant-R Distributed Amplifiers

A second technique used to extend the power capability of the amplifier is the cascode FET arrangement (a common source FET driving a common gate FET). The cascode provides three advantages over a single common source FET as the active element of the distributed amplifier. First, there is an improvement in power capability since the output voltage swing of the amplifier is across the gate-drain junction of the common gate FET. In this case, the voltage swing may reach the gate-drain breakdown voltage of the device while in the case of a common source device it is limited by the gate-drain breakdown voltage less the negative voltage swing on the gate (6). Second, the output impedance of the common gate FET is much higher than that of the common source FET and therefore drain line attenuation is much lower (7). Finally, the transmission line lengths between the common source and common gate FET's are very effective design elements in tuning the gain response of the amplifier for optimum gain flatness.

The third technique used to increase the power-bandwidth product of the circuit

is the "gate capacitor" (CG in figure 1) which is placed in series with the gate of each input FET (1,3). This technique enables one to increase the FET periphery of a distributed amplifier without losing bandwidth since the series capacitor-FET combination may be designed to have the same capacitance and gain as a single FET but with much greater periphery. In the case of this amplifier, the gate capacitors are approximately equal to the FET capacitance and therefore permit twice the gate periphery of a comparable design without gate capacitors.

The amplifier's single supply bias network is also novel. As shown in figure 5 a voltage divider is used to bias the gate of the common gate FET's while an external source resistor is used to bias the common source FET's. Gate-source voltages and drain-source voltages of the common source and common gate FET's are equalized when the gate voltage of the common gate FET is .46*VDD based on an operating gate-source voltage of -0.8V and an operating drain-source voltage of 4.6V.



$$V_{G2} = |V_{GS1}| + V_{DS1} - |V_{GS2}| = V_{DS1} = V_{DS2}$$

$$V_{DD} = |V_{GS1}| + V_{DS1} + V_{DS2} = 2V_{DS} + |V_{GS1}|$$

$$\frac{V_{G2}}{V_{DD}} = \frac{V_{DS}}{2V_{DS} + |V_{GS}|} = 0.46$$ for typical values of V_{GS} and V_{DS}

Figure 5. Bias Network of the Distributed Amplifier

A photograph of the amplifier appears in figure 6. This design utilizes eight 500 micron FET's (four common source and four common gate) with 0.5 micron gate lengths. Efforts at size reduction and a unique approach to R.F. grounding result in the compact design that measures 1.0 mm by 1.4 mm. With wraparound grounding, ground connections are restricted to the edge of the die so two grounded lines are used to R.F. bypass the sources of the common source FET's and the gates of the common gate FET's, respectively, to ground. Since D.C. bias must also be applied to these terminals another line runs on top of each ground line with the lines separated by a thin layer of silicon nitride. By widening the pairs of lines this combination serves as both an R.F. bypass capacitor and a low impedance path to ground. A key advantage of this method is that it allows one to use otherwise wasted space for bypass capacitors and thus decrease total chip area.

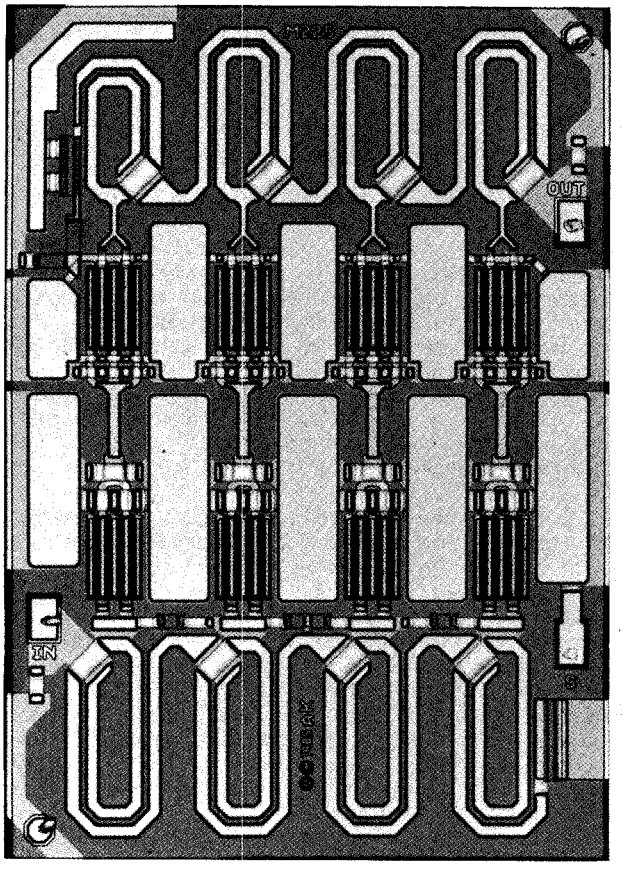


Figure 6. Photograph of the Distributed Amplifier

Predicted gain performance of this MMIC as simulated on Touchstone(tm) appears in figure 7. Since only pairs of coupled lines can be modeled some inaccuracies exist in the circuit model due to coupling within the bridged-tee coils and between adjacent coils. Also, since the bypass capacitors have four instead of the traditional two ports they cannot be modeled exactly but instead are modeled by two lumped capacitors at the edges of the chip.

Circuit Fabrication and Performance

Five wafers of this design were fabricated using an ion implant process

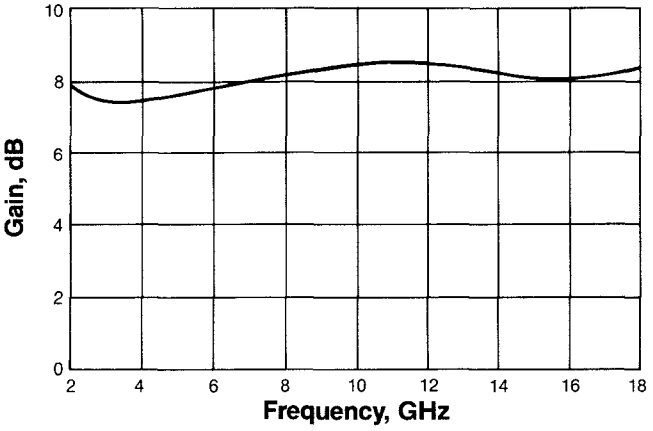


Figure 7. Predicted Gain of the Distributed Amplifier

(7). A typical part has an average gain of 6dB, a gain flatness of ±1dB and a minimum 1dB compressed power of 22dBm over the 2 to 18GHz band. R.F. performance is reasonably uniform with the highest gain wafer having an average gain of 8dB and the highest power wafer having minimum 1dB compressed power of 23dBm. Data measured from a typical device biased at 8V, 200mA is shown in figures 8a-d. All measurements were made on 15 mil thick alumina substrates.

The main discrepancy between simulated and measured performance is the gain rolloff at high frequencies which is caused by two factors. First, the coupled line used in the bridged-tee coil is more inductive than expected. This is due to an over-estimation of the internal coupling within the coil. Also, the transmission lines between the common source and common gate FET's appear less inductive than designed. This second factor is most likely due to the close proximity of these lines to the ground

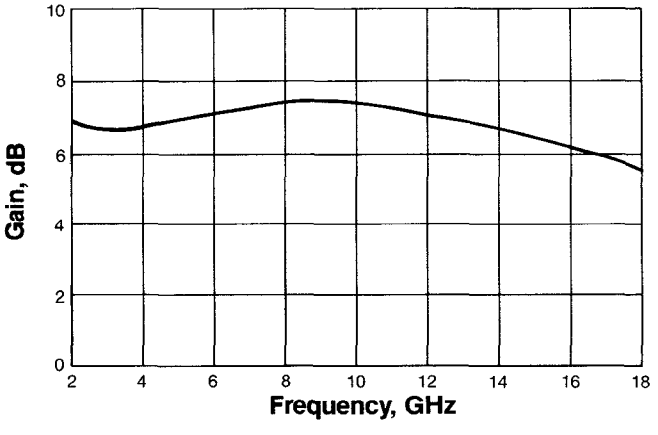


Figure 8a. Measured Gain of a Typical Distributed Amplifier

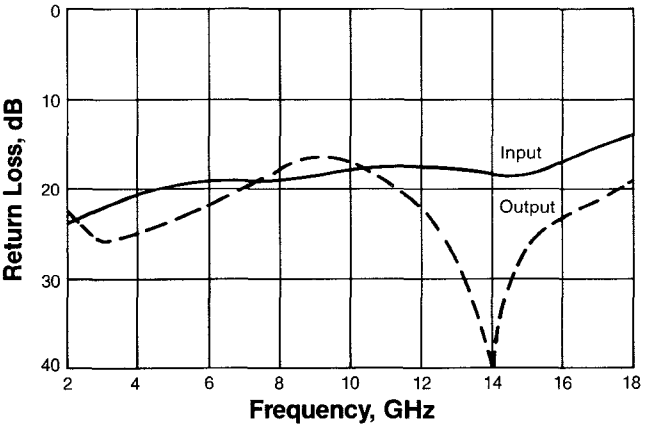


Figure 8b. Measured Input and Output Return Loss of a Typical Distributed Amplifier

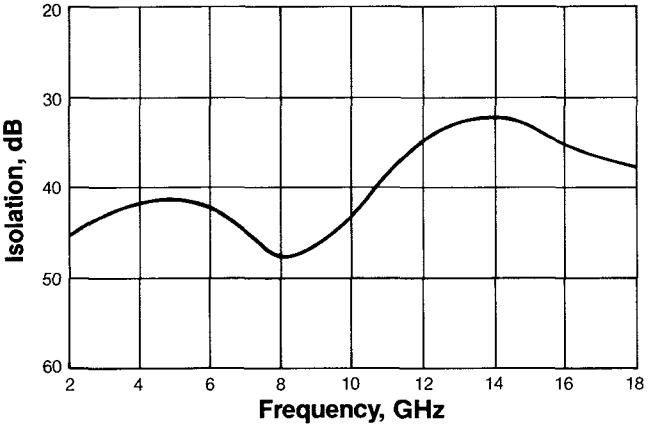


Figure 8c. Measured Isolation of a Typical Distributed Amplifier

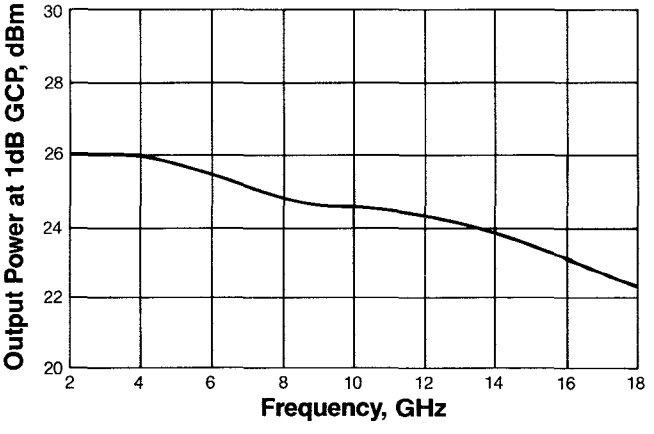


Figure 8d. Measured 1db Compressed Power of a Typical Distributed Amplifier

plates of the bypass capacitors and the capacitance of the four crossovers. Both of these elements may be corrected in a future mask set to improve the performance of this design.

Conclusions

The circuit techniques employed in this distributed amplifier have made possible a compact design that provides medium output power capability from 2 to 18 GHz. The constant-R network significantly improves the bandwidth of this design. Although this amplifier's performance does not agree perfectly with predicted performance, it has been analyzed to identify the causes of the discrepancy.

References

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